SESSION 18 – TAPA I
Advanced Metal Gate Materials

Thursday, June 17, 10:20 a.m.
Chairpersons: M. Mirabedini, LSI Logic
T. Ipplish, Renesas

18.1 — 10:20 a.m.

Dual Workfunction Fully Silicided Metal Gates, C. Cabral, Jr, J. Kedzierski, B. Linder, S. Zafar, V. Narayanan, S. Fang, A. Steegen, P. Kozlowski, R. Carruthers and R. Jammy, IBM SRDC, Yorktown Heights, NY and * IBM Microelectronics Division, Hopewell Junction, NY

Fully silicided (FUSI), dual workfunction, Ni monosilicide metal gates are demonstrated using Sb predoped polySi for setting the nFET workfunction and for the first time a combination of Al predoped polySi and a Ni(Pt) alloy silicide for the pFET workfunction. The combination of the Sb and Al predoped polySi along with the Ni(Pt)Si, allow for workfunctions spanning the Si band gap to within 0.2 eV of the band edges. This process is applicable for both high performance and low power CMOS applications.

18.2 — 10:45 a.m.

Thermally Robust Dual-Work Function ALD-MN_x MOSFETs Using Conventional CMOS Process Flow, D.-G. Park, Z.J. Luo, N. Edleman, W. Zhu, P. Nguyen, K. Wong, C. Cabral*, P. Jamison*, B.H. Lee, A. Chou, M. Chudzik, J. Bruley, O. Gluschenkov, P. Ronsheim, A. Chakravarti, R. Mitchell, V. Ku, H. Kim*, E. Duch*, P. Kozlowski*, C. D'Emic*, V. Narayanan*, A. Steegen, R. Wise, R. Jammy*, R. Rengarajan, H. Ng, A. Sekiguchi and C.H. Wann, IBM SRDC, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY

Thermally stable dual work function metal gates are demonstrated using a conventional CMOS process flow. The gate structure consists of poly-Si/metalnitrides (MNx)/ SiON (or high-k)/Si stack with atomic layer deposition (ALD)-TaNx for the NFET and ALD-WNx for the PFET. Much enhanced drive current (Id) and transconductance (Gm) values, and reduced off current characteristics were attained with ALD-MNx gated devices over control poly-Si and PVD-MNx devices within controllable Vt shifts.

18.3 — 11:10 a.m.

Laminated Metal Gate Electrode with Tunable Work Function for Advanced CMOS, S.H. Bae, W.P. Bai, H.C. Wen, S. Mathew*, L.K. Bera*, N. Balasubramanian*, N. Yamada**, M.F. Li*** and D.L. Kwong, University of Texas, Austin, TX, *Institute of Microelectronics, Singapore, **ANELVA Corporation, Tokyo, Japan, ***National University of Singapore, Singapore

Laminated metal gate electrodes consisting of 1~3 ultra thin (~10 Å) layers and bulk metal nitride gate electrodes were deposited, followed by RTP annealing to evaluate their thermal stability. Through lamination, TiTaNx alloy gate is formed which exhibits NMOS compatible work function (4.35 eV) with good thermal stability up to 900 C. Laminated metal gates consisting of 3 components exhibit MOS compatible work function (5.0~5.2 eV) after 1000 C annealing, which remains unchanged after subsequent thermal processing

18.4 — 11:35 a.m.

Demonstration of Fully Ni-Silicided Metal Gates on HfO_2 Based High-k Gate Dielectrics as a Candidate for Low Power Applications, K.G. Anil, A. Veloso, S. Kubicek, T. Schram, E. Augendre, J.-F. de Marneffe, K. Devriendt, A. Lauwers, S. Brus, K. Henson and S. Biesemans, Interuniversity Microelectronics Center, Leuven, Belgium

We have fabricated fully Ni-silicided metal gate (FUSI) CMOS devices with HfO2-based gate dielectrics for the first time. We demonstrate that full silicidation eliminates the Fermi level pinning at the polySi-HfO2 dielectric interface in pFETs. For nMOS devices, a 5 orders of magnitude reduction in short channel sub-threshold leakage is obtained with similar drive current compared to the poly gate devices. In addition, the FUSI process does not degrade the hysterisis nor the dielectric breakdown. This result makes FUSI on high-K a strong candidate for scaled low power technologies.

18.5 — 12:00 p.m.

Dual Work Function Metal Gate CMOS using CVD Metal Electrodes, V. Narayanan, A. Callegari, F.R. McFeely, K. Nakamura**, P. Jamison, S. Zafar, E. Cartier, A. Steegen*, V. Ku*, P. Nguyen*, K. Milkove, C. Cabral Jr., M. Gribelyuk*, C. Wajda**, Y. Kawano**, D. Lacey, Y. Li*, E. Sikorski, E. Duch, H. Ng*, C. Wann*, R. Jammy, M. Ieong* and G. Shahidi, , IBM SRDC, Yorktown Heights, NY, *IBM, Hopewell Junction, NY, **Tokyo Electron America (TEL), Hopewell Junction, NY

Dual workfunction metal gated MOSFETs with low damage CVD processes for TaSiN, W and Re have been fabricated on HfO2. Tinv as low as 1.46 nm with appropriate Vts and sub-threshold slopes 90 mV/decade or better have been achieved. Excellent hole mobility has been obtained and electron mobility optimization is shown to critically depend on specific electrode and interface layer combinations along with post deposition processing even for nominally identical HfO2 layers.